What is claimed is:

1. A clock generating device, comprising:

a clock producing section to produce plural clocks differing in phase; and

a selecting section to select and output a first clock from the plural clocks and to switch from the first clock to a second clock having a phase or a cycle period each differing from that of the first clock during a period that the first clock is being outputted.

2. The clock generating device of claim 1, further comprising:

a switching control section to output a selection signal to indicate which clock to be selected to the selecting section.

3. The clock generating device of claim 2, wherein the switching control section is structured so as to judge whether or not the first clock is switched to the clock having a phase or a cycle period each differing from that of the first clock during a period that the first clock is being outputted.

4. The clock generating device of claim 2, wherein the switching control section is structured so as to produce the selection signal based on predetermined output clock information.

5. The clock generating device of claim 4, further comprising:

a memory section to store the output clock information.

6. The clock generating device of claim 4, further comprising:

a calculating section to calculate the output clock information.

7. The clock generating device of claim 1, wherein the clock generating device is structured by an integral circuit.

8. The clock generating device of claim 7, wherein the clock generating device is structured by a digital circuit.

9. The clock generating device of claim 2, further comprising:

an entire control section to control an entire of the clock generating device.

10. The clock generating device of claim 9, further comprising:

a control counter section to produce region information to indicate a region to be switched to the second clock based on region data received by the entire control section and the switching control section produces the selection signal based on the region information.

11. The clock generating device of claim 1, wherein the clock producing section comprises a reference clock generating section to generate a reference clock and a delay chain section to produce plural different delay clocks based on the reference clock.

12. The clock generating device of claim 11, further comprising:

a synchronous signal detecting section to detect a number of stages of a delay clock synchronizing with the reference clock from the plural different delay clocks.

13. A clock generating device, comprising:

a reference clock generating section to generate a reference clock;

a delay chain section to produce plural delay clocks showing different delay conditions respectively based on the reference clock;

a synchronous signal detecting section to detect a number of stages of a delay clock synchronizing with the reference clock from the plural delay clocks and to produce synchronous information;

an entire control section to control an entire of the clock generating device and to produce output clock information and region data;

a control counter section to produce based on the region data region information indicating a region where a first clock is changed to a second clock having a phase or a cycle period each differing from that of the first clock among the plural delay clocks;

a switching control section to output a selection signal based on the reference clock outputted from the reference clock generating section, the synchronous information outputted from the synchronous signal detecting section, the output clock information outputted from the entire control section, and the region information outputted from the control counter section; and

a selecting section to select and output the first clock and to switch from the first clock to a second clock

within a predetermined time period based on the selection signal outputted from the switching control section.

14. A base board, comprising:

the clock generating device of claim 1.

15. An image forming apparatus, comprising:

the clock generating device of claim 1; and

a writing device to write an image based on the clock outputted from the select section;

wherein the writing device writes an image to be located in a predetermined region based on the second clock and an image to be located outside of the predetermined region based on the first clock.

16. A clock generating device, comprising:

a delay chain section including plural delay elements connected in a form of a chain so as to produce a delay clock delayed from a reference clock;

a synchronous signal detecting section to select plural delay clocks synchronizing with a leading reference clock and to derive synchronous information corresponding to a delay stage number of one cycle from the selected plural delay clocks;

a select section to select a synchronous clock synchronizing with a reference clock from the delay chain section by referring the synchronous information derived from the synchronous signal detecting section;

a switching control section to disperse time intervals between clock signals by conducting alternately for each optional clock the selection of the synchronous clock in the selecting section and the selection of the delay clock from the delay chain section in a way to add an optional time.

17. The clock generating device of claim 16, wherein the select section conduct the selection of the synchronous clock and the selection of the delay clock alternately for each clock.

18. The clock generating device of claim 16, wherein the clock generating device is structured by an integral circuit.

19. The clock generating device of claim 18, wherein the clock generating device is structured by a digital circuit.

20. An image forming apparatus, comprising:

the clock generating device of claim 16,

the image forming apparatus controlled by clock outputted from the clock generating device.

21. A clock generating device, comprising:

a delay chain section including plural delay elements connected in a form of a chain so as to produce a delay clock delayed from a reference clock;

a synchronous signal detecting section to select plural delay clocks synchronizing with a leading reference clock and to derive synchronous information corresponding to a delay stage number of one cycle from the selected plural delay clocks;

a select section to select a synchronous clock synchronizing with a reference clock from the delay chain section by referring the synchronous information derived from the synchronous signal detecting section;

a switching control section to disperse time intervals between clock signals by conducting alternately for each optional clock the selection of the synchronous clock in the selecting section and the selection of the delay clock from the delay chain section in a way to subtract an optional time.

22. The clock generating device of claim 21, wherein the select section conduct the selection of the synchronous clock and the selection of the delay clock alternately for each clock.

23. The clock generating device of claim 21, wherein the clock generating device is structured by an integral circuit.

24. The clock generating device of claim 23, wherein the clock generating device is structured by a digital circuit.

25. An image forming apparatus, comprising:

the clock generating device of claim 21,

the image forming apparatus controlled by clock outputted from the clock generating device.

26. A clock generating device, comprising:

a delay chain section including plural delay elements connected in a form of a chain so as to produce a delay clock delayed from a reference clock;

a synchronous signal detecting section to select plural delay clocks synchronizing with a leading reference clock and to derive synchronous information corresponding to a delay

stage number of one cycle from the selected plural delay clocks;

a select section to select a synchronous clock synchronizing with a reference clock from the delay chain section by referring the synchronous information derived from the synchronous signal detecting section;

a switching control section to disperse time intervals between clock signals by conducting alternately for each optional clock the selection of the synchronous clock in the selecting section, the selection of the delay clock from the delay chain section in a way to add an optional time and the selection of the delay clock from the delay chain section in a way to subtract an optional time.

27. The clock generating device of claim 26, wherein the select section conduct the selection of the synchronous clock and the selection of the delay clock alternately for each clock.

28. The clock generating device of claim 26, wherein the clock generating device is structured by an integral circuit.

29. The clock generating device of claim 27, wherein the clock generating device is structured by a digital circuit.

30. An image forming apparatus, comprising:

the clock generating device of claim 26,

the image forming apparatus controlled by clock outputted from the clock generating device.

31. A clock generating method, comprising steps of:

producing delay clocks by delaying a reference clock by plural delay elements connected in a form of a chain;

deriving synchronous information corresponding to a delay stage number of one cycle by selecting plural delay clocks synchronizing with a leading reference clock from the delay clocks; and

conducting alternately for each predetermined time period a first selection of the synchronous clock synchronizing with a reference clock and a second selection of the delay clock directed so as to add an optional time for the synchronous clock by referring the synchronous information.